

**Amendments to the Claims**

The claims are unamended. The currently pending claims are listed below.

1. (Previously Presented) A digital data processing system, comprising:
  - 2 a memory;
  - 3 at least one processor having at least one associated cache for temporarily caching data
  - 4 from said memory;
  - 5 at least one device having a device cache, said device cache having a fixed number of slots
  - 6 for caching data, said fixed number being greater than one, each slot caching a cache line of data;
  - 7 and
  - 8 a cache coherency mechanism, said cache coherency mechanism including a cache line
  - 9 state directory structure, said cache coherency mechanism selectively determining whether to send
  - 10 cache line invalidation messages to said at least one device using state information in said cache
  - 11 line state directory structure, wherein at least a portion of said cache line state directory structure
  - 12 associated with said at least one device contains exactly said fixed number of cache line entries,
  - 13 each entry having a fixed correspondence to a unique respective one of said fixed number of slots
  - 14 for caching data of said device cache.
  
1. 2. (Original) The digital data processing system of claim 1, wherein said device is an I/O
- 2 bridge device.

1       3. (Previously Presented) The digital data processing system of claim 1, wherein a processor  
2 portion of said cache line state directory structure contains cache line state for at least one said  
3 cache associated with a processor, said processor portion being separate from said at least a  
4 portion of said cache line state directory structure associated with said at least one device, said  
5 processor portion containing a plurality of cache line entries, each entry having a fixed  
6 correspondence to a respective set of real addresses, said cache coherency mechanism further  
7 selectively determining whether to send cache line invalidation messages to the processor with  
8 which the cache is associated using state information in said processor portion of said cache line  
9 directory structure.

1       4. (Original) The digital data processing system of claim 3, wherein said processor portion  
2 of said cache line state directory structure contains cache line state for a plurality of caches  
3 associated with a plurality of processors, said cache coherency mechanism further selectively  
4 determining whether to send cache line invalidation messages to any of said plurality of  
5 processors using state information in said processor portion of said cache line directory structure.

1       5. (Original) The digital data processing system of claim 1, wherein said digital data  
2 processing system comprises a plurality of nodes, each node containing at least one processor, a  
3 respective portion of said memory, and a respective portion of said cache coherency mechanism.

1       6. (Original) The digital data processing system of claim 5, wherein each said respective  
2 portion of said cache coherency mechanism in each respective node maintains cache line state  
3 information for cached data having a real address in the respective portion of said memory  
4 contained in the node.

1       7. (Original) The digital data processing system of claim 5, wherein each said respective  
2       portion of said cache coherency mechanism in each respective node maintains cache line state  
3       information for data cached in devices contained in the node.

1       8. (Previously Presented) The digital data processing system of claim 1,  
2       wherein said digital data processing system comprises a plurality of devices having  
3       respective device caches, each said device cache having a respective fixed number of slots for  
4       caching data, each slot caching a cache line of data; and

5       wherein said cache line state directory structure includes a plurality of portions, each  
6       portion corresponding to a respective one of said plurality of devices, each portion containing a  
7       respective fixed number of cache line entries equal to said respective fixed number of slots for  
8       caching data of the device cache to which the respective portion corresponds, each entry  
9       corresponding to a unique respective one of the respective fixed number of slots for caching data  
10      of the device cache to which the respective portion corresponds.

1       9. (Previously Presented) A method for maintaining cache coherency in a digital data  
2       processing system, comprising the steps of:

3               maintaining a cache line state directory structure, said cache line state directory structure  
4       having at least a portion corresponding to a device cache in a device of said digital data  
5       processing system, said portion containing exactly N cache line entries, wherein N is a fixed  
6       number greater than one, each entry having a fixed correspondence to a unique respective one of  
7       N slots for caching lines of data in said device cache, said device cache containing exactly N slots  
8       for caching N lines of data;

9               responsive to each of a plurality of data access requests, accessing said cache line state  
10      directory structure to determine whether data having a data address referenced by the request is  
11      contained in said device cache;

12               for each of said plurality of data access requests, determining whether to send an  
13      invalidation message to said device based on whether said step of accessing said cache line state  
14      directory determines that data having a data address referenced by the request is contained in said  
15      device cache; and

16               for each of said plurality of data access requests, sending an invalidation message to said  
17      device responsive to the determination made by said step of determining whether to send an  
18      invalidation message.

1       10. (Original) The method of claim 9, wherein said device is an I/O bridge device.

1 11. (Original) The method of claim 9, further comprising the steps of:

2 receiving a plurality of data access requests for cache lines of data from said device, each  
3 data access request from said device including data identifying a slot of said device cache in  
4 which the cache line will be stored; and

5 responsive to receiving each said data access request from said device, updating said cache  
6 line state directory structure by writing cache line identifying information corresponding to the  
7 data access request at the entry corresponding to the slot in which the cache line requested by the  
8 data access request will be stored.

1 12. (Original) The method of claim 9, wherein said step of maintaining a cache line state  
2 directory structure comprises maintaining a first portion of said cache line state directory structure  
3 corresponding to said device cache, and a second portion of said cache line state directory  
4 structure corresponding to a plurality of caches associated with a plurality of processors, said  
5 method further comprising the steps of:

6 responsive to each of said plurality of data access requests, accessing said cache line state  
7 directory structure to determine whether data having a data address referenced by the request is  
8 contained in any of said plurality of processors;

9 for each of said plurality of data access requests, determining whether to send an  
10 invalidation message to any of said plurality of processors based on whether said step of accessing  
11 said cache line state directory structure determines that data having a data address referenced by  
12 the request is contained in any of said plurality of processors; and

13 for each of said plurality of data access requests, sending an invalidation message to at least  
14 one of said plurality of processors responsive to the determination made by said step of  
15 determining whether to send an invalidation message to any of said plurality of processors.

1       13. (Original) The method of claim 9, wherein said digital data processing system comprises  
2       a plurality of nodes, each node containing at least one processor, a respective portion of said  
3       memory, and a respective portion of said cache coherency mechanism.

1       14. (Previously Presented) A digital data processing system, comprising:  
2            a memory;  
3            a plurality of processors controlling a plurality of caches for temporarily caching data from  
4       said memory;  
5            at least one device having a device cache, said device cache having a fixed number of slots  
6       for caching data, each slot for storing a cache line; and  
7            a cache line state directory structure having a first portion for maintaining cache line state  
8       for lines of data cached in said plurality of caches controlled by said plurality of processors, and a  
9       second portion for maintaining cache line state for lines of data cached in said device cache;  
10       wherein said first portion of said cache line state directory structure contains a plurality of  
11       cache line entries, each entry having a fixed correspondence to a respective set of real addresses;  
12       wherein said second portion of said cache line state directory structure contains exactly  
13       said fixed number of cache line entries, each entry having a fixed correspondence to a unique  
14       respective one of said fixed number of slots for caching data of said device cache.

1       15. (Original) The digital data processing system of claim 14, wherein said device is an I/O  
2       bridge device.

1       16. (Original) The digital data processing system of claim 14, wherein said digital data  
2       processing system comprises a plurality of nodes, each node containing at least one processor, a  
3       respective portion of said memory, and a respective portion of said cache line state directory  
4       structure.

1 17. (Original) The digital data processing system of claim 16, wherein each said respective  
2 portion of said cache line state directory structure each respective node contains cache line state  
3 information for cached data having a real address in the respective portion of said memory  
4 contained in the node.

1 18. (Original) The digital data processing system of claim 16, wherein each said respective  
2 portion of said cache line state directory structure each respective node contains cache line state  
3 information for data cached in devices contained in the node.

1 19. (Previously Presented) A cache coherency apparatus for a digital data processing system:  
2 a communications interface for communicating with a plurality of devices;  
3 a cache line state directory structure, wherein at least a portion of said cache line state  
4 directory structure corresponds to a cache having exactly N slots for caching data in a first device  
5 of said plurality of devices, wherein N is a fixed number greater than one, said at least a portion  
6 containing exactly N cache line entries, each entry having a fixed correspondence to a unique  
7 respective one of said N slots for caching data of said cache in said first device; and  
8 cache coherence control logic which selectively generates invalidation messages responsive  
9 to events affecting the validity of cached data, said cache coherence control logic determining  
10 whether to send cache line invalidation messages to said first device using state information in  
11 said at least a portion of said cache line state directory structure corresponding to said cache in  
12 said first device.

1 20. (Original) The cache coherency apparatus of claim 19, wherein said first device is an I/O  
2 bridge device.

1        21. (Previously Presented) The cache coherency apparatus of claim 19, wherein said cache  
2        line state directory structure contains a plurality of discrete portions, including a first portion  
3        corresponding to said cache in said first device, and a second portion corresponding to at least one  
4        cache associated with a processor, said second portion containing a plurality of cache line entries,  
5        each entry having a fixed correspondence to a respective set of real addresses, said cache  
6        coherence control logic further selectively determining whether to send cache line invalidation  
7        messages to said processor using state information in said second portion of said cache line state  
8        directory structure.

1        22. (Original) The cache coherency apparatus of claim 19, wherein said cache coherency  
2        apparatus is embodied in a single integrated circuit chip, said integrated circuit chip being  
3        separate from said first device.